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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/801,564	03/08/2001	Ashley Saulsbury	016747014610	5355

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EXAMINER

DO, CHAT C

ART UNIT	PAPER NUMBER
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2124

DATE MAILED: 05/20/2004

9

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/801,564

Applicant(s)

SAULSBURY ET AL.

Examiner

Chai C. Do

Art Unit

2124

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 March 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4-13 and 15-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,4-13 and 15-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date. _____ | 6) <input type="checkbox"/> Other: _____ |

Art Unit: 2124

DETAILED ACTION

1. This communication is responsive to Amendment A, filed 03/03/2004.
2. Claims 1-2, 4-13, and 15-24 are pending in the application. Claims 1, 9, and 18 are independent claims. In Amendment A, claims 1, 4-6, 8-9, and 17-18 are amended, claims 3 and 14 are cancelled, and claims 23-24 are added. This action is made final.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the new limitations just added to independent claims (e.g. the second operands are equal in value to an immediate value wherein the immediate value is specified in an instruction) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-2, 4-8, and 23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 1, the limitation "the intermediate value is specified in an instruction that identifies the first source register" in lines 6-7 is unclear whether the intermediate value and the first source register are specified in the instruction or only the intermediate value is specified in an instruction. For examination purposes, the examiner considers the limitation above as the intermediate value is specified in an instruction only.

Thus, claims 2, 4-8, and 23 are also rejected for being dependent on the rejected base claim 1.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-7, 18, and 21-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin et al. (U.S. 5,959,874).

Re claim 1, Lin et al. disclose in Figures 4a, 7, 9, 12, and 16-17 a processing core comprising: a first source register including a plurality of first operands a plurality of second operands (SRC1, SRC2 and abstract); wherein the plurality of second operands are equal in value to an immediate value (throughout the specification, Lin et al. do not

disclose the second operands in SRC2 are different nor the same. Therefore, all the elements/operands in SRC2 can set to be equal in value), and the immediate value is specified in an instruction (e.g. Figure 7a. the instruction in 702 specifies SRC1 and SRC2 wherein SRC2 including an immediate value) that identifies the first source register; a bit-wise inverter coupled to at least one of the first plurality of operands and the second plurality of operands (1603 in Figure 16); a destination register including a plurality of results (DEST in abstract and col. 2 lines 55-59); a plurality of arithmetic processors (907a-907h in Figure 9) respectively coupled to the first operands (Source1), second operands (Source2) and results (910a-910h in Figure 9), wherein each arithmetic processor computes one of a sum and a difference of the first operand and a respective second operand (either addition or subtraction in Figure 9).

Re claim 2, Lin et al. further disclose in Figures 4a, 7, 9, 12, and 16-17 comprising an integrated circuit which includes the first source register, destination register and arithmetic processor (source1, source2, and destination in Figure 9 and col. 2 lines 55-59).

Re claim 4, Lin et al. further disclose in Figures 4a, 7, 9, 12, and 16-17 each arithmetic processor computes at least one of: the result of the first operand plus another operand plus the intermediate (1706 in Figure 17); and the result of the first operand minus another operand minus the intermediate value.

Re claim 5, Lin et al. further disclose in Figures 4a, 7, 9, 12, and 16-17 the immediate value is signed (Figure 5b).

Re claim 6, Lin et al. further disclose in Figures 4a, 7, 9, 12, and 16-17 a prescaler which scales the immediate value (703 in Figure 7a as saturation applied).

Re claim 7, Lin et al. further disclose in Figures 4a, 7, 9, 12, and 16-17 a first width of the first source register is a positive integer multiple of a second width of the first operand (abstract lines 5-6 and Figure 5b).

Re claim 18, Lin et al. disclose in Figures 4a, 7, 9, 12, and 16-17 a method for performing arithmetic processing, comprising the steps of-loading loading a first and second operands from a primary source register (702 in Figure 7a as SRC1); loading an immediate value (702 in Figure 7a as SRC2) that has a value expressly specified in an instruction (e.g. Figure 7a. the instruction in 702 specifies SRC1 and SRC2 wherein SRC2 including an immediate value); performing an arithmetic function on the first operand and immediate value to produce a first result (bits 7-0 in Figure 7a); performing the arithmetic function on the second operand and immediate value to produce a second result (bits 15-8 in Figure 7a); and storing the first and second results in a destination register (706 in Figure 7a).

Re claim 21, Lin et al. further disclose in Figures 4a, 7, 9, 12, and 16-17 the two performing steps are performed, at least partially, coextensive in time (Figure 9).

Re claim 22, Lin et al. further disclose in Figures 4a, 7, 9, 12, and 16-17 comprising a step of adjusting at least one of the first and second results to avoid saturation of the destination register (703 in Figure 7a as saturation applied).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 8 and 19-20 are rejected under 35 U.S.C. 103(a) as being obvious over Lin et al. (U.S. 5,959,874).

Re claim 8, Lin et al. disclose in Figures 4a, 7, 9, 12, and 16-17 the sum and the difference are performed on the same adder. Lin et al. do not disclose the adder is carry look-ahead. However, the examiner takes an official notice that the carry look-ahead adder is well known in the art that is widely used in multiple simultaneous adders. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to use the carry look-ahead adder in Lin et al.'s invention because it would enable to increase the system performance by reducing the propagation delay.

Re claims 19-20, Lin et al. do not disclose the immediate value has a width of nine or thirteen bits. However, it is obvious to application choice to have the immediate value has a width of nine or thirteen bits. Therefore, it would have been obvious application to a person having ordinary skill in the art at the time the invention is made to have the width of the immediate value of nine or thirteen bits in Lin et al.'s invention because it would enable to reduce the system circuitry for a particular application.

10. Claims 9-17 are rejected under 35 U.S.C. 103(a) as being obvious over Lin et al. (U.S. 5,959,87) in view of Wang (U.S. 6,243,730).

Re claim 9, Lin et al. disclose in Figures 4a, 7, 9, 12, and 16-17 a method for performing arithmetic processing, the method comprising the steps of: loading a first and second operands from a primary source register (702 in Figure 7a as SRC1); loading a third and fourth operands (702 in Figure 7a as SRC2); wherein the third and fourth operands are an immediate value specified in an instruction (e.g. Figure 7a. the instruction in 702 specifies SRC1 and SRC2 wherein SRC2 including an immediate value), and the third and fourth operands are equal in value (throughout the specification, Lin et al. do not disclose the second operands in SRC2 are different nor the same. Therefore, all the elements/operands in SRC2 can set to be equal in value); scaling the third and fourth operands according to a predetermined scaling factor (703 in Figure 7a as saturation applied). Lin et al. do not disclose a step of performing an arithmetic function on the first and third operands to produce a first result; performing the arithmetic function on the second and fourth operands to produce a second result; and storing the first and second results in a destination register. However, Wang discloses in Figure 7 a step of performing an arithmetic function on the first and third operands to produce a first result ($A_{real} * B_{real} = C_{real}$); performing the arithmetic function on the second and fourth operands to produce a second result ($A_{image} * B_{image} = C_{image}$); and storing the first and second results in a destination register (C_{real} and C_{image} in Figure 7). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add steps of performing an arithmetic function on the first and third

operands to produce a first result; performing the arithmetic function on the second and fourth operands to produce a second result; and storing the first and second results in a destination register as seen in Wang's invention into Lin et al.'s invention because it would enable to reduce the circuitry and increase the system performance in performing complex operation.

Re claim 10, Lin et al. further disclose in Figures 4a, 7, 9, 12, and 16-17 comprising a step of inverting the third and fourth operands (714a and 714b in Figure 7b).

Re claim 11, Lin et al. further disclose in Figures 4a, 7, 9, 12, and 16-17 further comprising a step of adjusting at least one of the first and second results to avoid saturation of the destination register (703 in Figure 7a as saturation applied).

Re claim 12, Lin et al. further disclose in Figures 4a, 7, 9, 12, and 16-17 wherein the step of performing an arithmetic function on the first and third operands comprises calculating the first operand plus the second operand plus a positive integer (addition in Figure 9 and saturate).

Re claim 13, Lin et al. further disclose in Figures 4a, 7, 9, 12, and 16-17 wherein the step of performing an arithmetic function on the second and fourth operands comprises calculating the second operand minus the fourth operand minus a positive integer (subtraction in Figure 9 and un/saturate).

Re claim 14, Lin et al. further disclose in Figures 4a, 7, 9, 12, and 16-17 wherein the third and fourth operands are the same immediate value (abstract).

Re claim 15, Lin et al. further disclose in Figures 4a, 7, 9, 12, and 16-17 wherein the predetermined scaling factor is divisible by two (col. 9 lines 1-8).

Re claim 16, Lin et al. further disclose in Figures 4a, 7, 9, 12, and 16-17 wherein the two performing steps are performed, at least partially, coextensive in time (Figure 9).

Re claim 17, it has the same limitation cited in claim 8. Thus, claim 17 is also rejected under the same rationale in the rejection of claim 8.

11. Claims 1 and 18 are rejected under 35 U.S.C. 103(a) as being obvious over Lin et al. (U.S. 5,959,87) in view of Mennemeier (U.S. 5,831,885).

Re claim 1, Lin et al. disclose in Figures 4a, 7, 9, 12, and 16-17 a processing core comprising: a first source register including a plurality of first operands a plurality of second operands (SRC1, SRC2 and abstract); a bit-wise inverter coupled to at least one of the first plurality of operands and the second plurality of operands (1603 in Figure 16); a destination register including a plurality of results (DEST in abstract and col. 2 lines 55-59); a plurality of arithmetic processors (907a-907h in Figure 9) respectively coupled to the first operands (Source1), second operands (Source2) and results (910a-910h in Figure 9), wherein each arithmetic processor computes one of a sum and a difference of the first operand and a respective second operand (either addition or subtraction in Figure 9). Even though Lin et al. do not explicitly disclose the plurality of second operands are equal in value to an immediate value and the immediate value is specified in an instruction that identifies the first source register. However, Mennemeier discloses in Figures 7 and 11a the plurality of second operands are equal in value to an immediate

value (e.g. first operand is equal to third operand and second operand is equal to fourth operand in 720 of Figure 7) and the immediate value is specified in an instruction (1112, 1114, and 1116 in Figure 11a) that identifies the first source register. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to have a plurality of second operands are equal in value and specified in an instruction as seen in Mennemeier's invention into Lin et al.'s invention because it would enable easily and efficiently to process multiple data on a constant (e.g constant coefficients) in image processing.

Re claim 18, Lin et al. disclose in Figures 4a, 7, 9, 12, and 16-17 a method for performing arithmetic processing, comprising the steps of-loading loading a first and second operands from a primary source register (702 in Figure 7a as SRC1); loading an immediate value (702 in Figure 7a as SRC2) performing an arithmetic function on the first operand and immediate value to produce a first result (bits 7-0 in Figure 7a); performing the arithmetic function on the second operand and immediate value to produce a second result (bits 15-8 in Figure 7a); and storing the first and second results in a destination register (706 in Figure 7a). Even though, Lin et al. do not explicitly disclose that a value expressly specified in an instruction. However, Mennemeier discloses in Figure 11a that a value expressly specified in an instruction (1112, 1114, and 1116 in Figure 11a). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to specify a value in an instruction as seen in Mennemeier's invention into Lin et al.'s invention because it would enable easily and efficiently to manipulate or modified the value for the plurality of second operands.

Response to Arguments

12. Applicant's arguments with respect to claims 1-2, 4-13, and 15-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

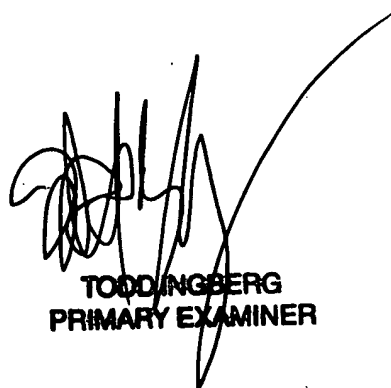
Art Unit: 2124

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2124

May 3, 2004



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PRIMARY EXAMINER